

Exponent: Arbitrary Bandwidth Receiver Architecture

Dana Sorensen; Colton Lindstrom; Jake Gunther

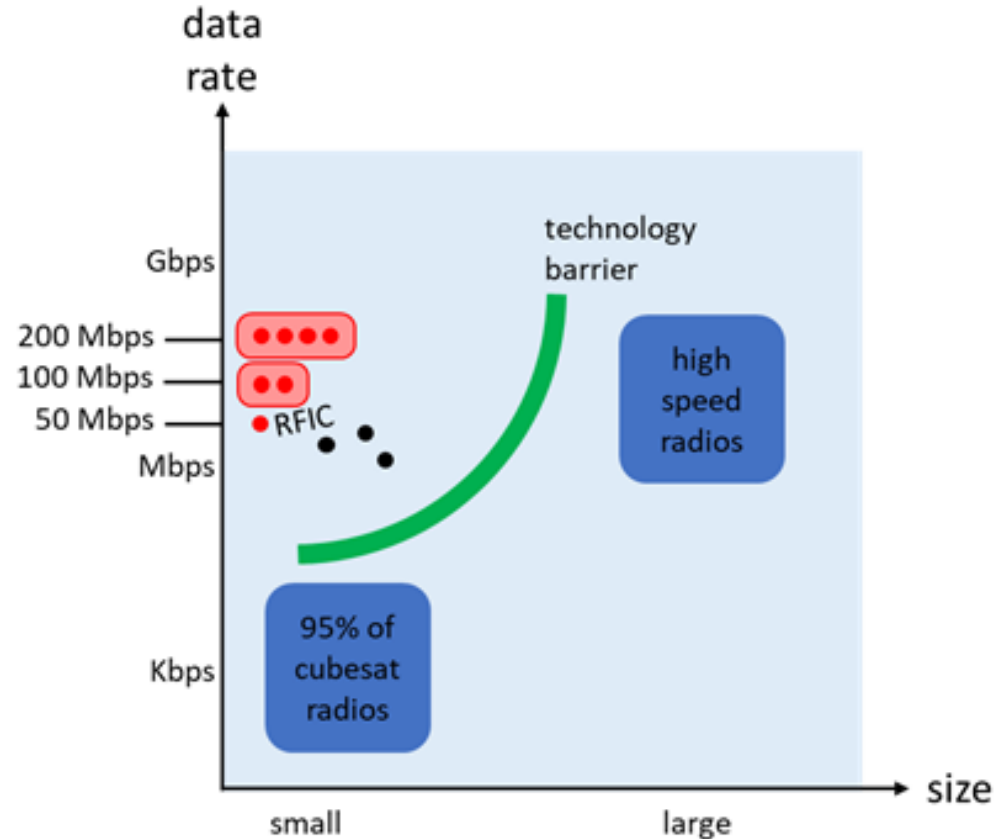
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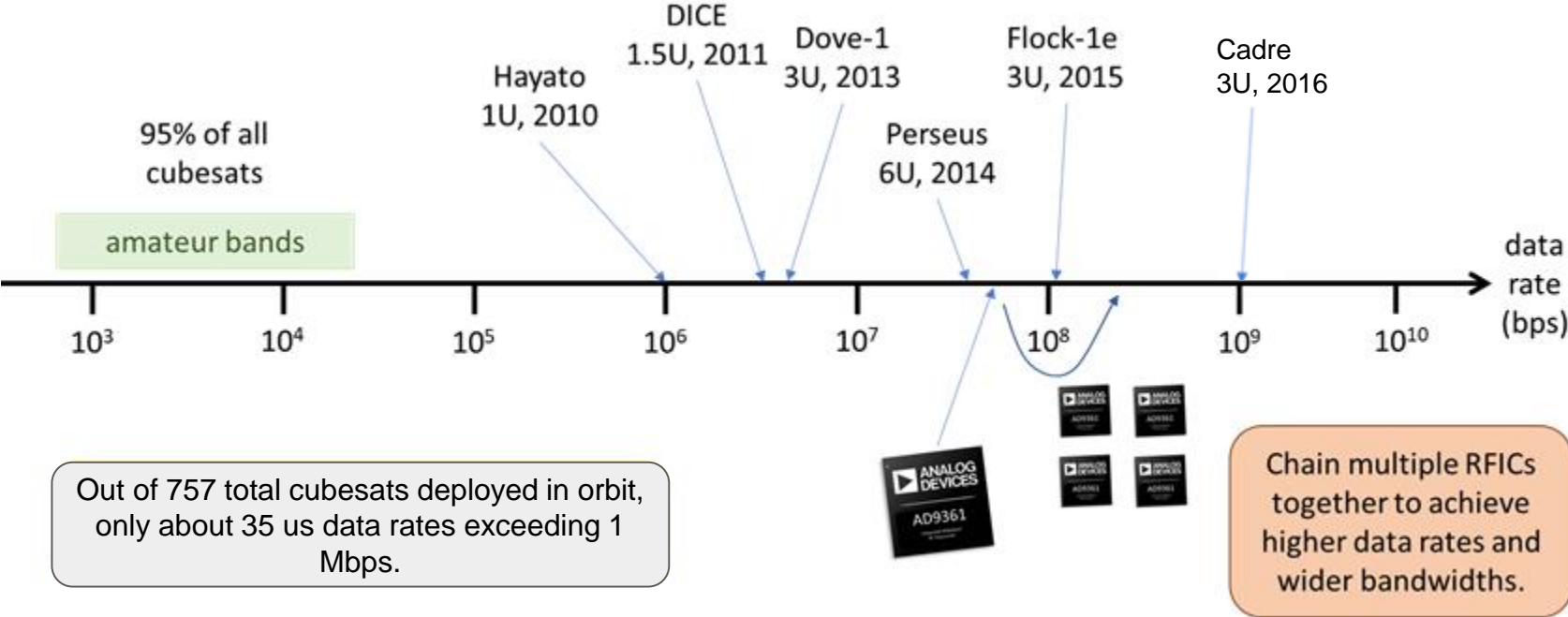
Background

Motivation

- Demand for high speed data transmission on CubeSats.
- Faster radios are larger, more expensive, and more power hungry.
- Chain multiple small radios together to achieve higher data rates.
- Leverage investment of telecommunications industry in RFICs.



Motivation

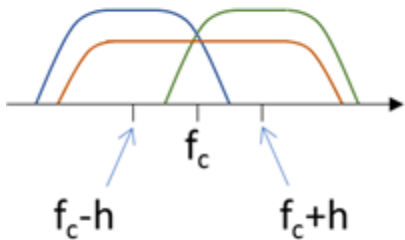


Out of 757 total cubesats deployed in orbit, only about 35 us data rates exceeding 1 Mbps.

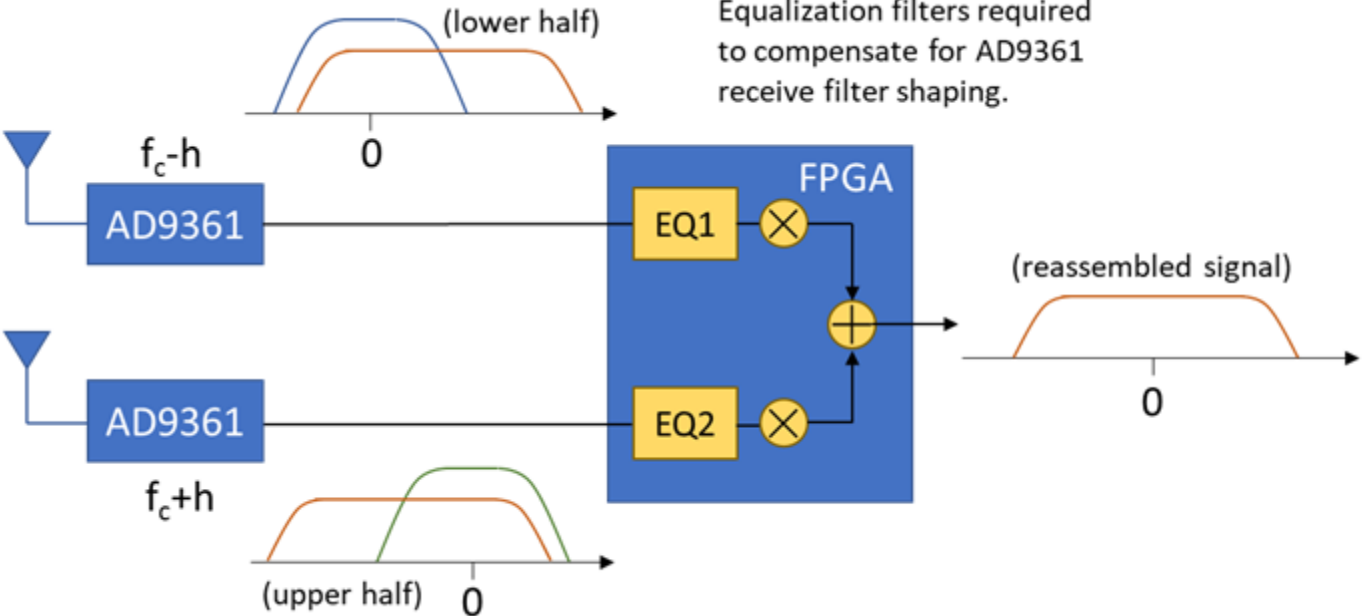
Chain multiple RFICs together to achieve higher data rates and wider bandwidths.

Concept

Desired signal too wide for one receiver.



Use two receivers. Each receiver tuned with a frequency offset.



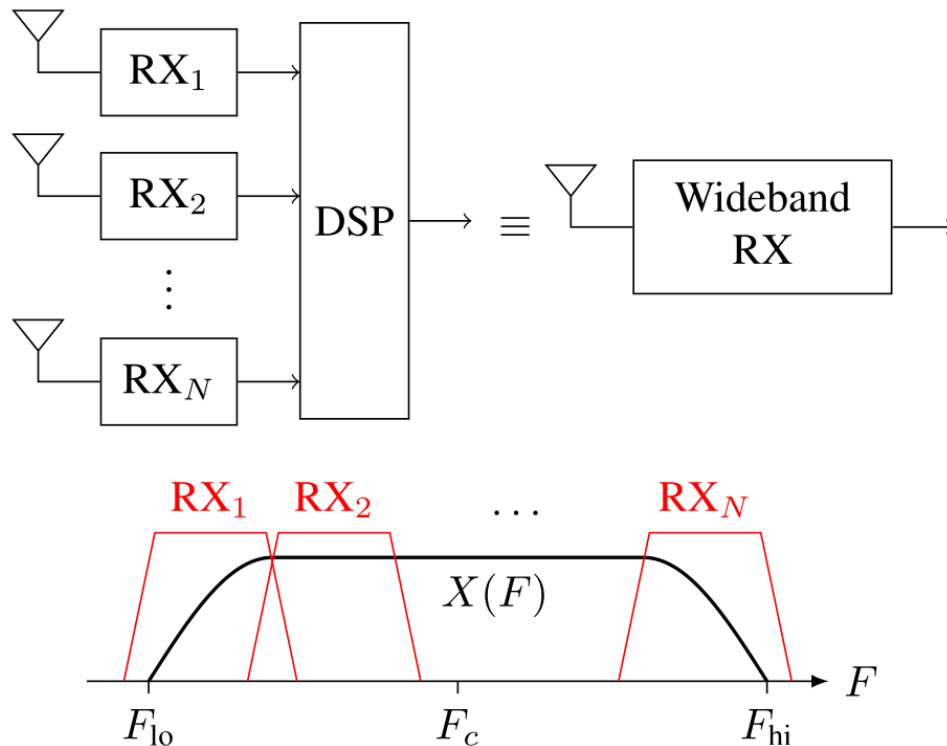
Theory and Simulation

Overview

Combine signals from more than one receiver to produce a single wide-band signal

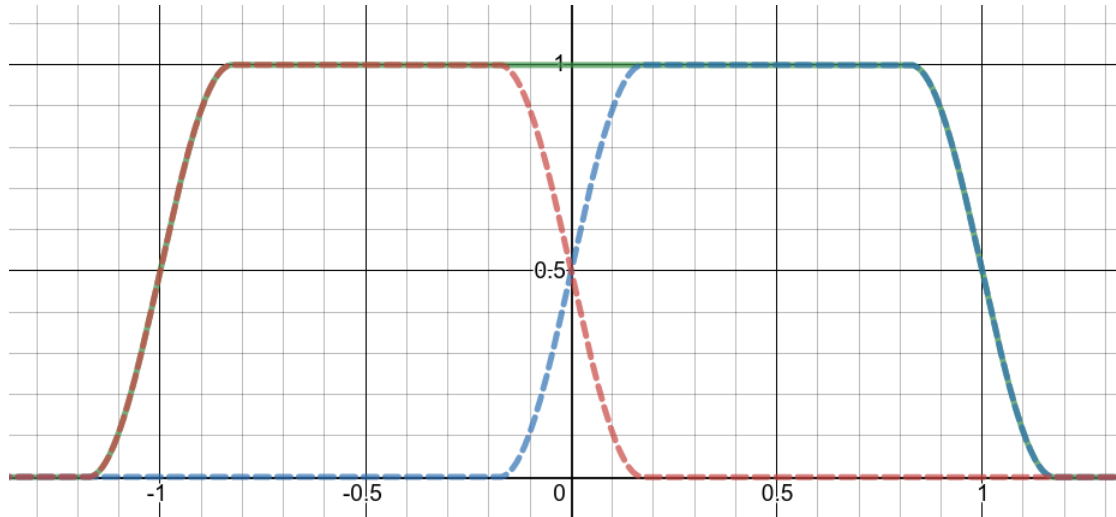
Any number of receivers can be used for an arbitrarily large bandwidth

Can this work in a general case, without shared LO?



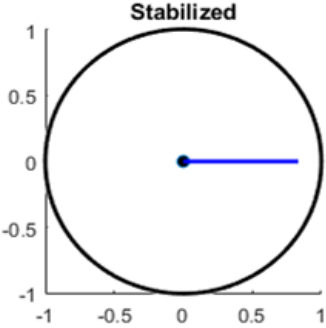
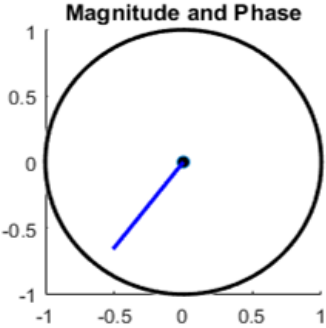
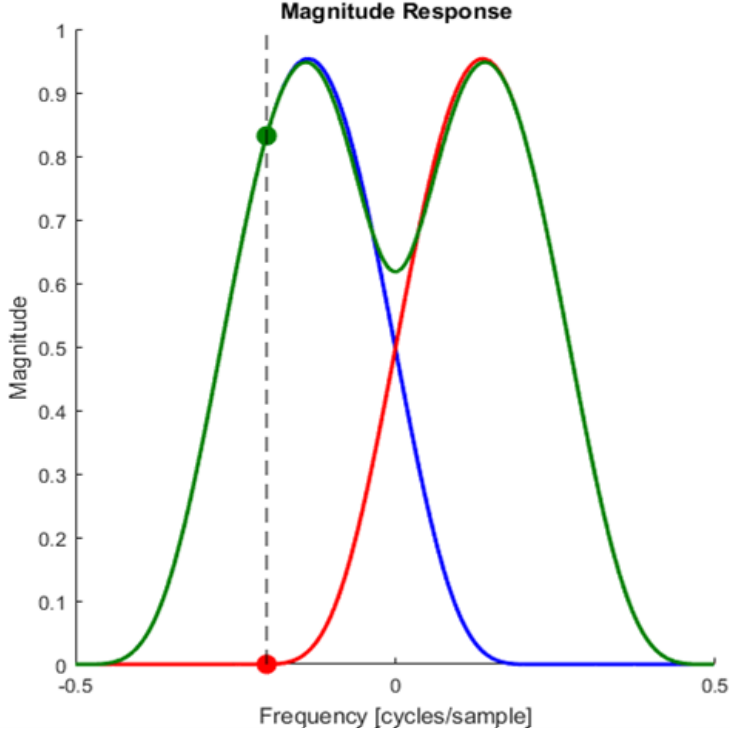
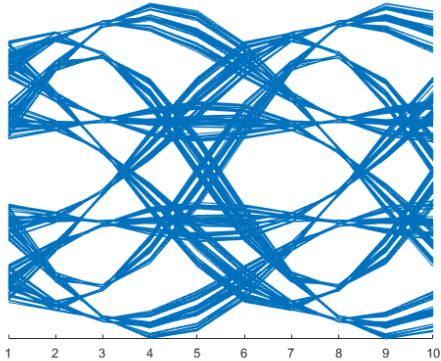
Shaping Filters

Nyquist filters (e.g. raised cosine) have the property that magnitudes of the overlapping region add to unity in the frequency domain.



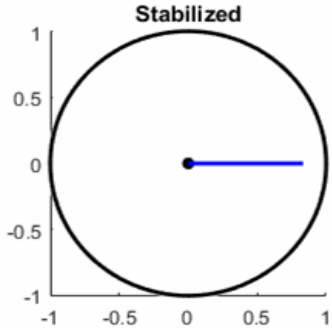
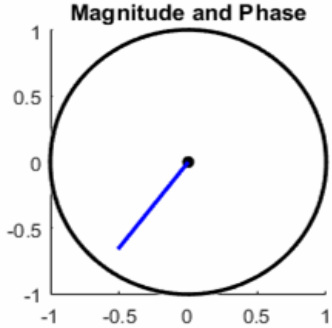
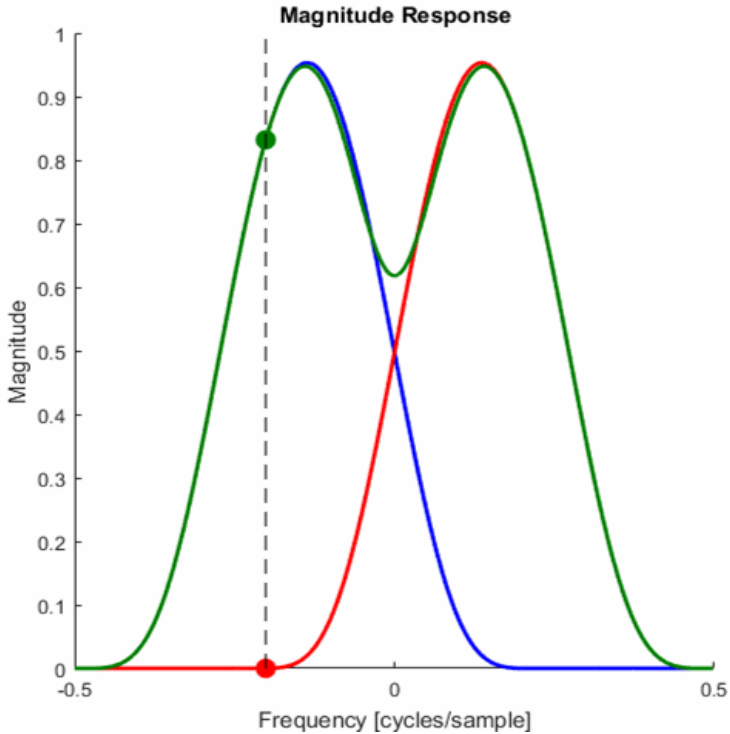
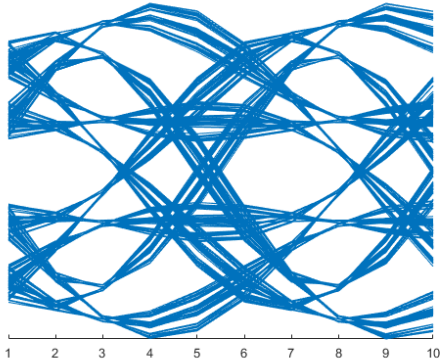
Signal Combination Without Phase Synchronization

Phase offsets cause distortion in the combined signal.



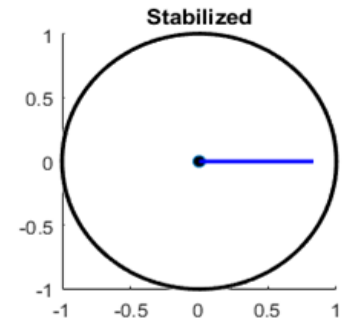
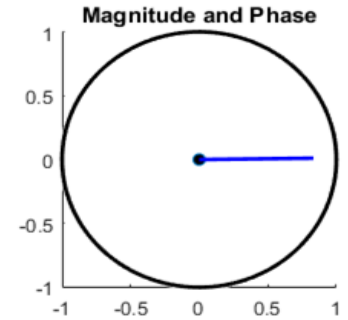
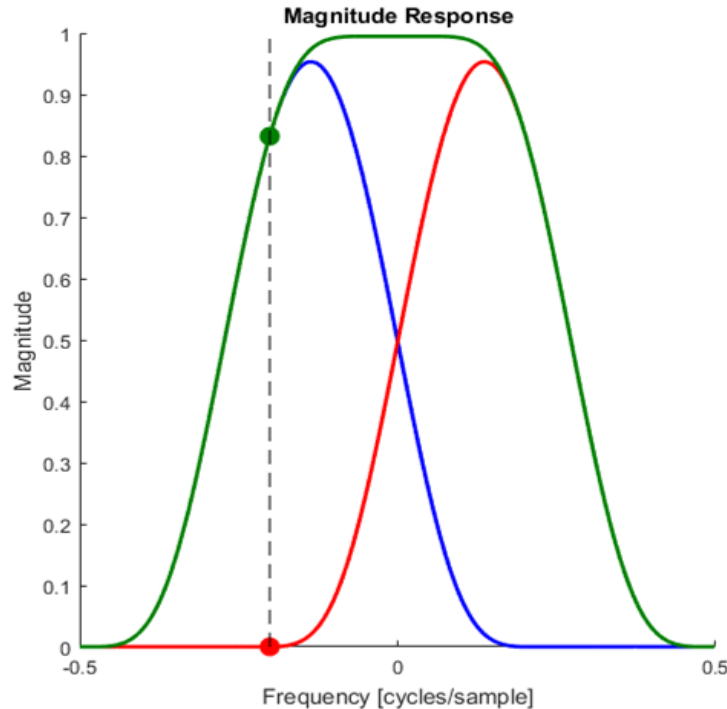
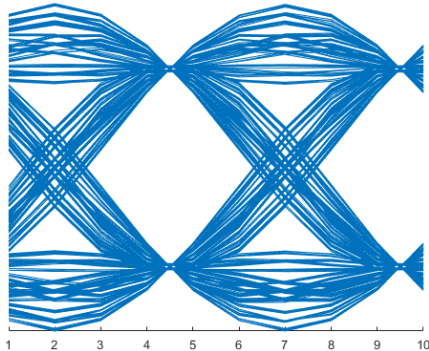
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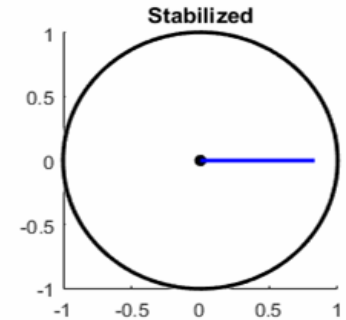
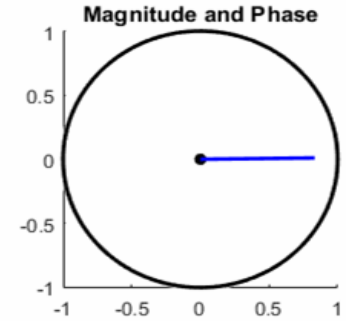
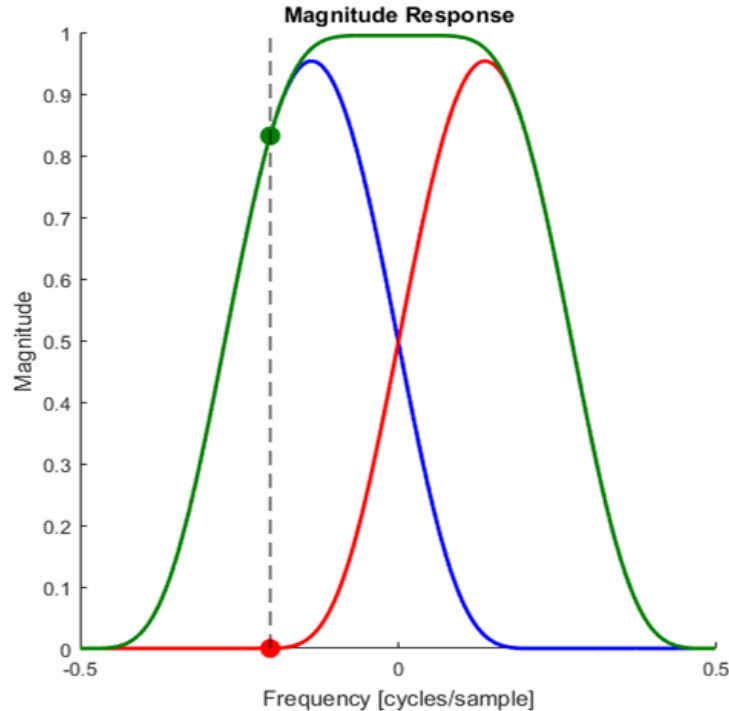
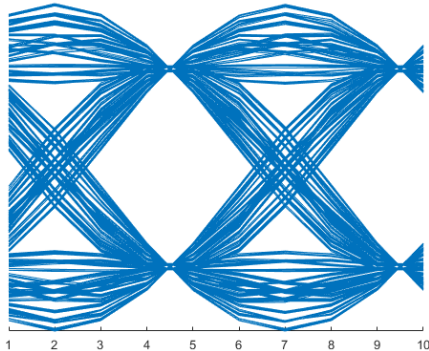
Signal Combination With Phase Synchronization

When components are phase aligned, they can be added to recreate the original signal.

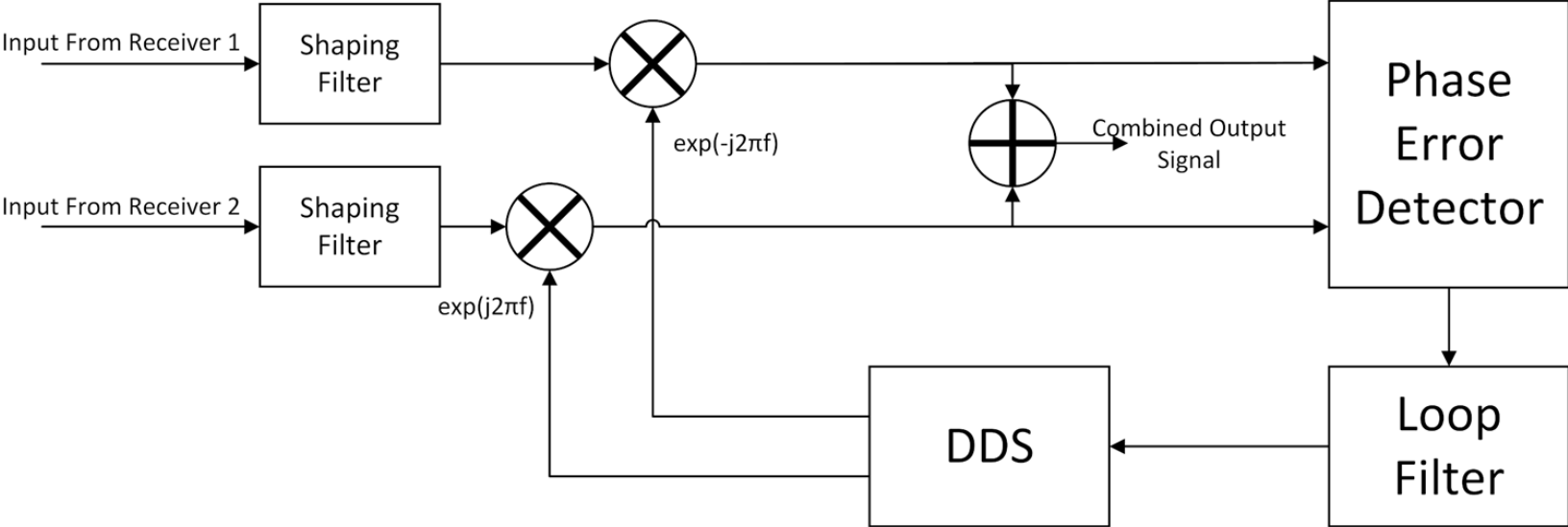


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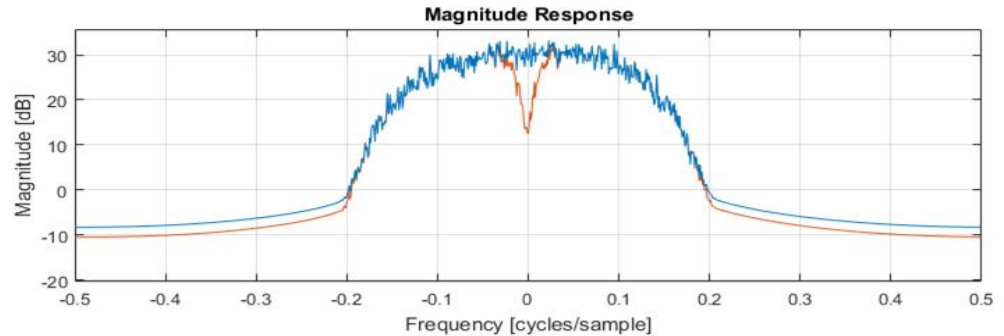
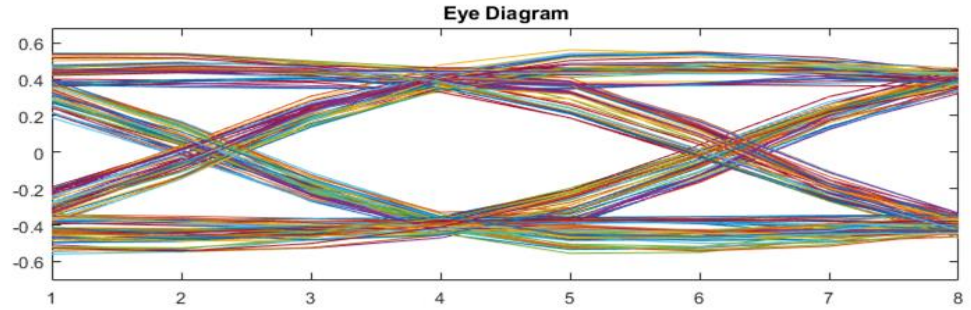
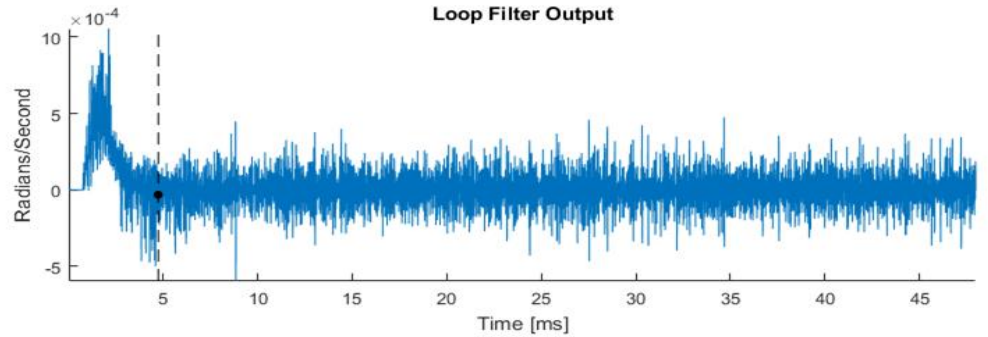


Phase Synchronization Architecture



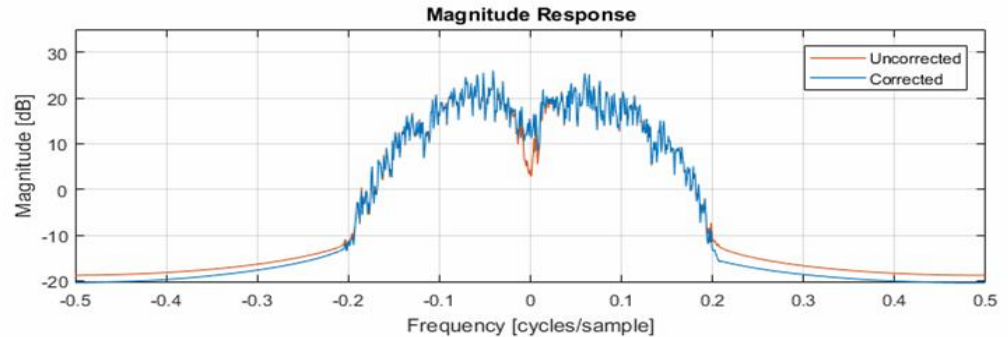
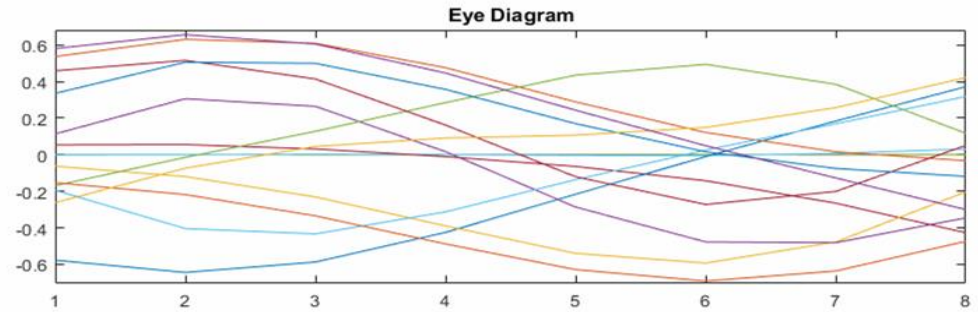
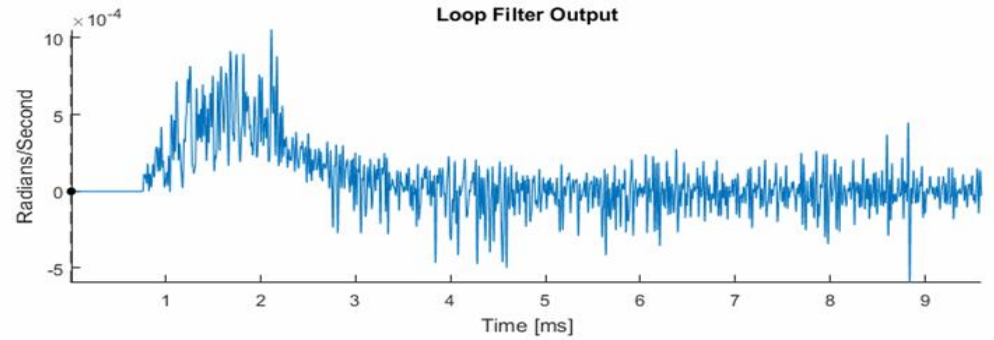
Phase Synchronization Results

- Sample signals collected from two AD9361 receivers
- Processed using MATLAB
- Quickly locks to signal



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Proof of Concept

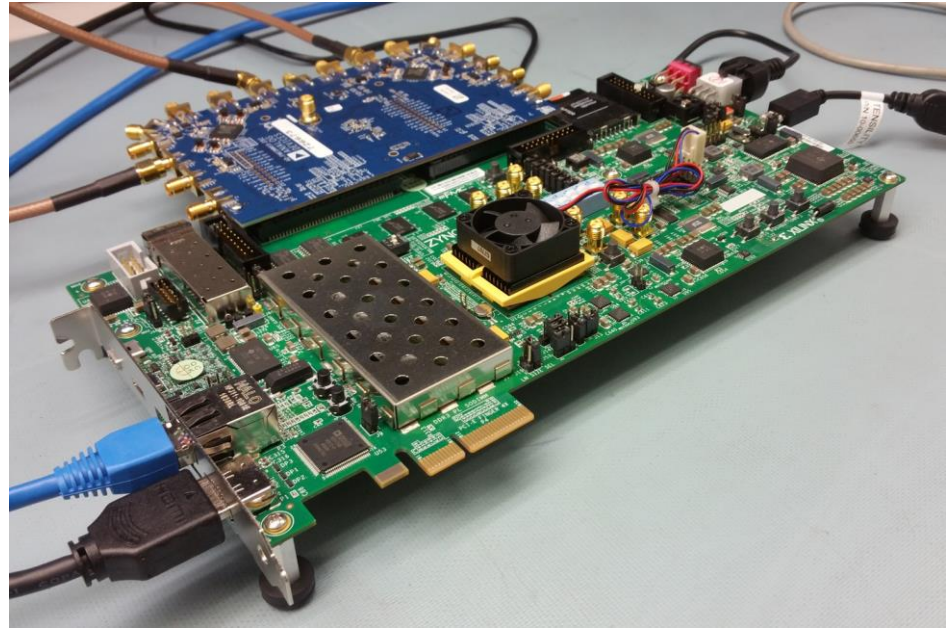
Hardware Implementation

AD FMCOMMS5

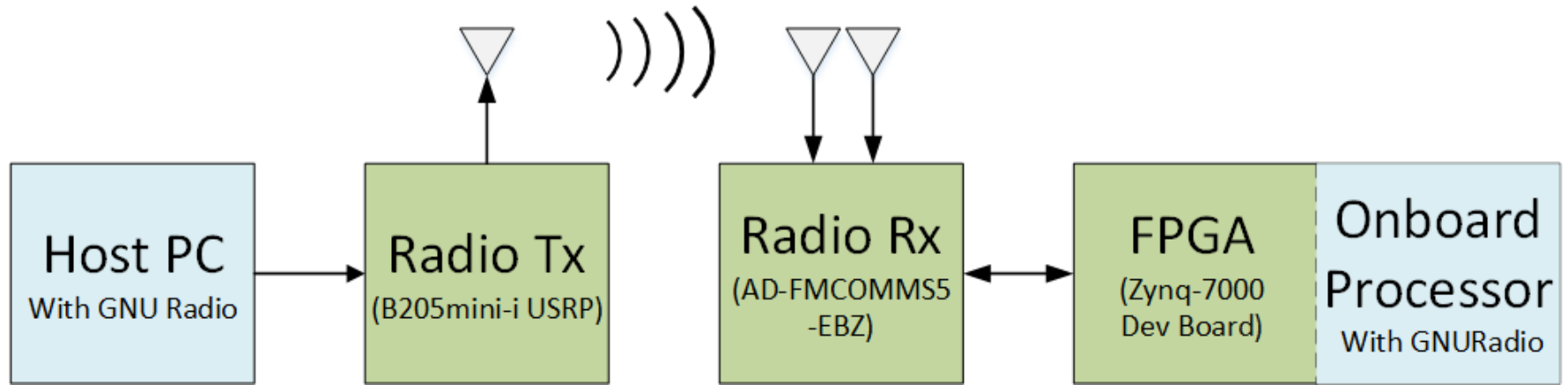
- Dual AD9361 RFICs
- 70 MHz - 6 GHz range
- Up to 56 MHz BW (each)
- Synchronized sampling
- Separate LOs (in our configuration)

Zync-7000 SoC

- Synchronization logic implemented on FPGA for real-time demonstration

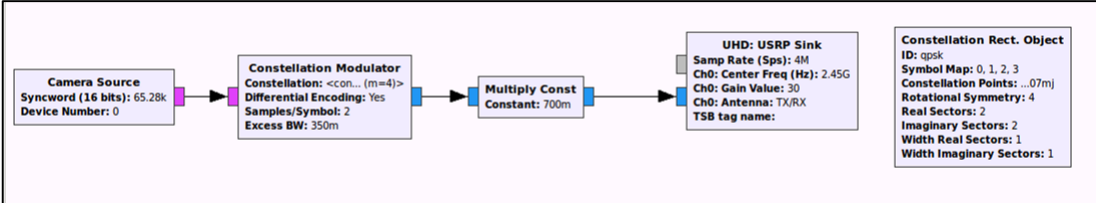


Hardware Implementation

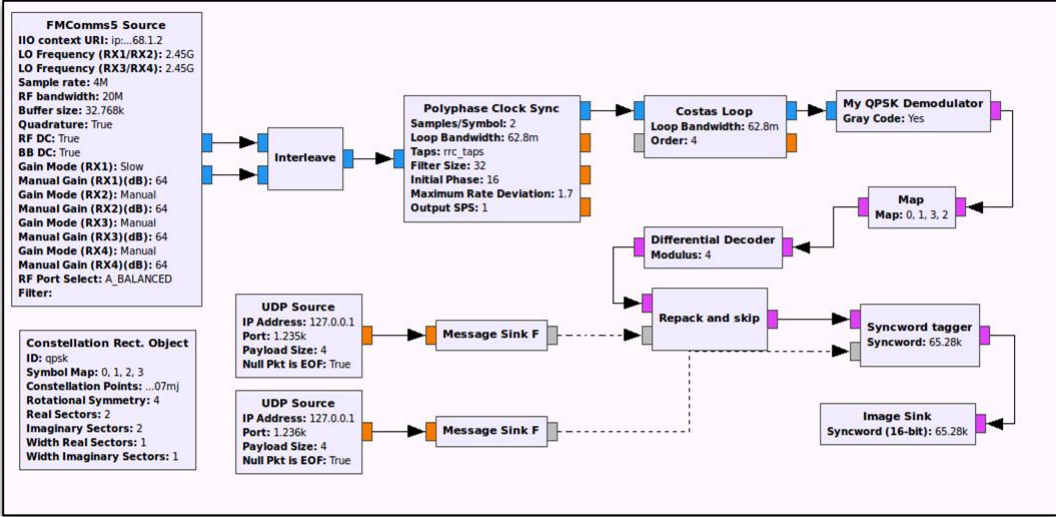


GNU Radio Transmit and Receive

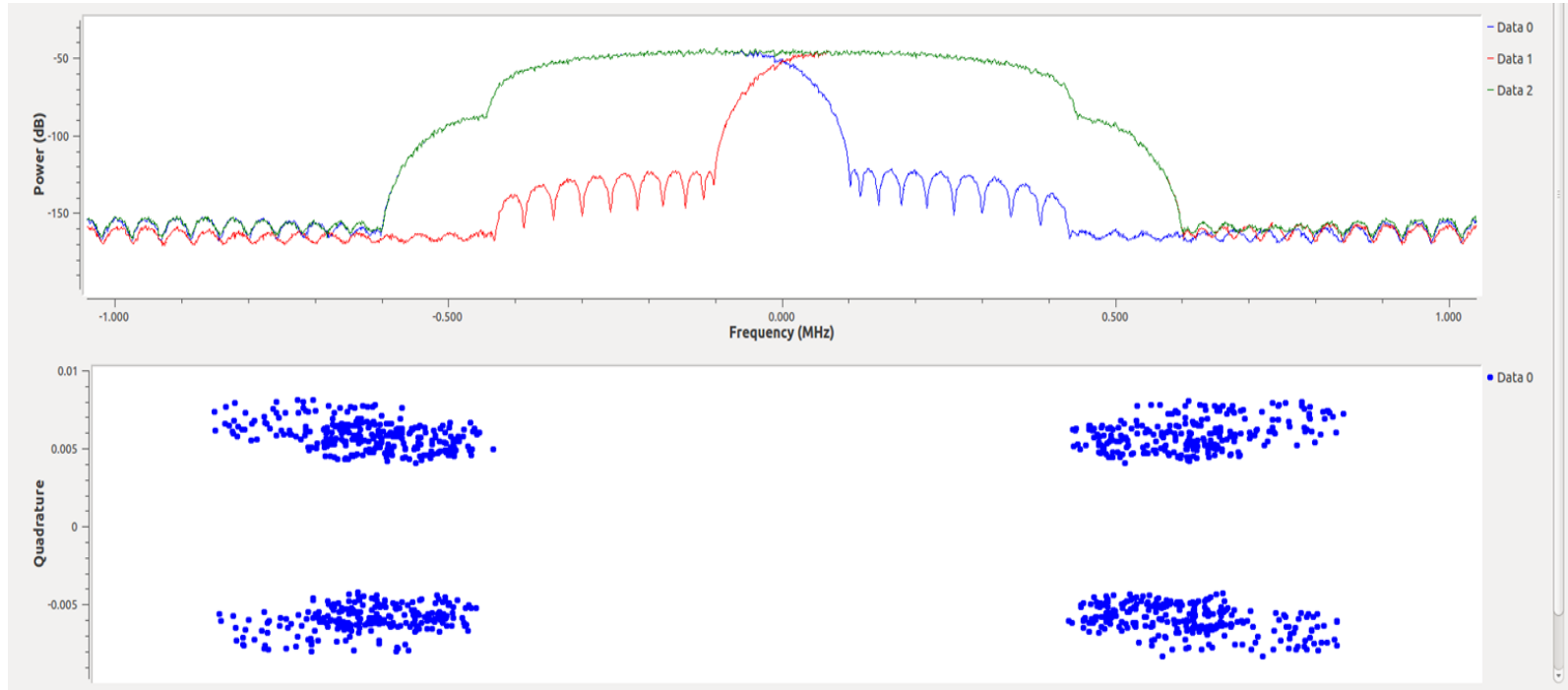
Transmit



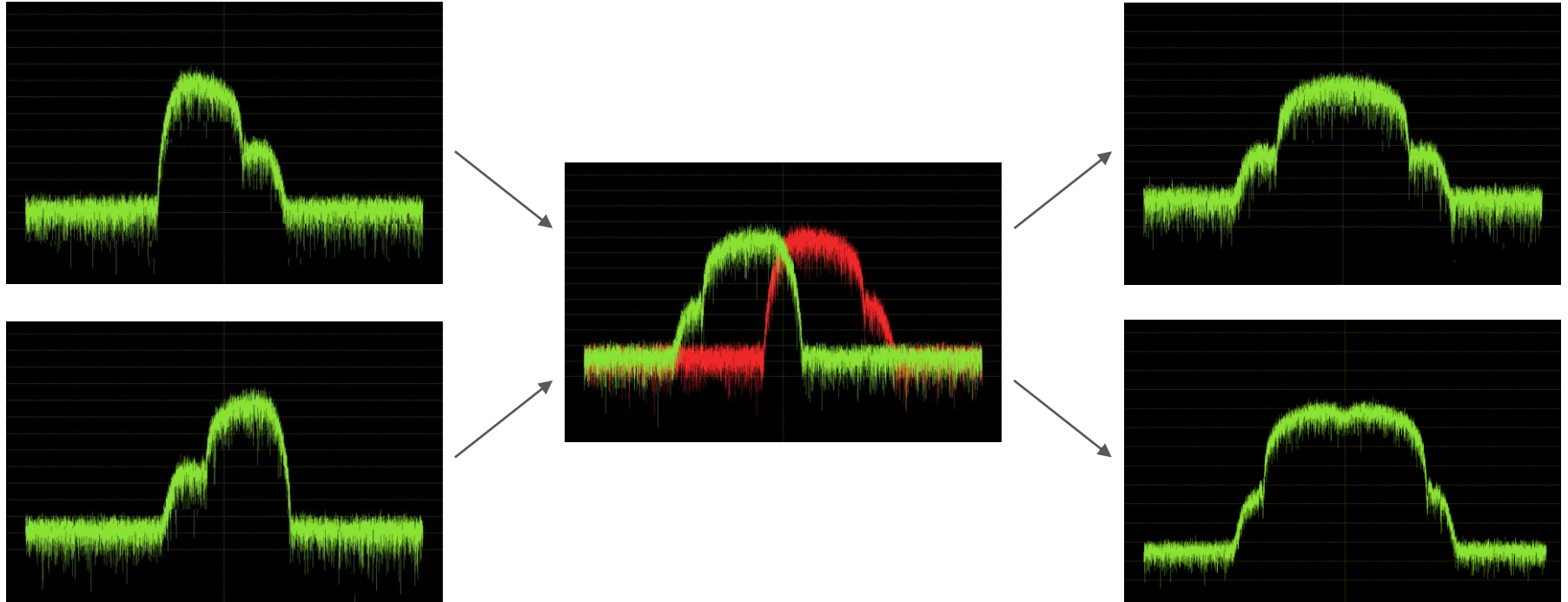
Receive



Synchronization in GNU Radio



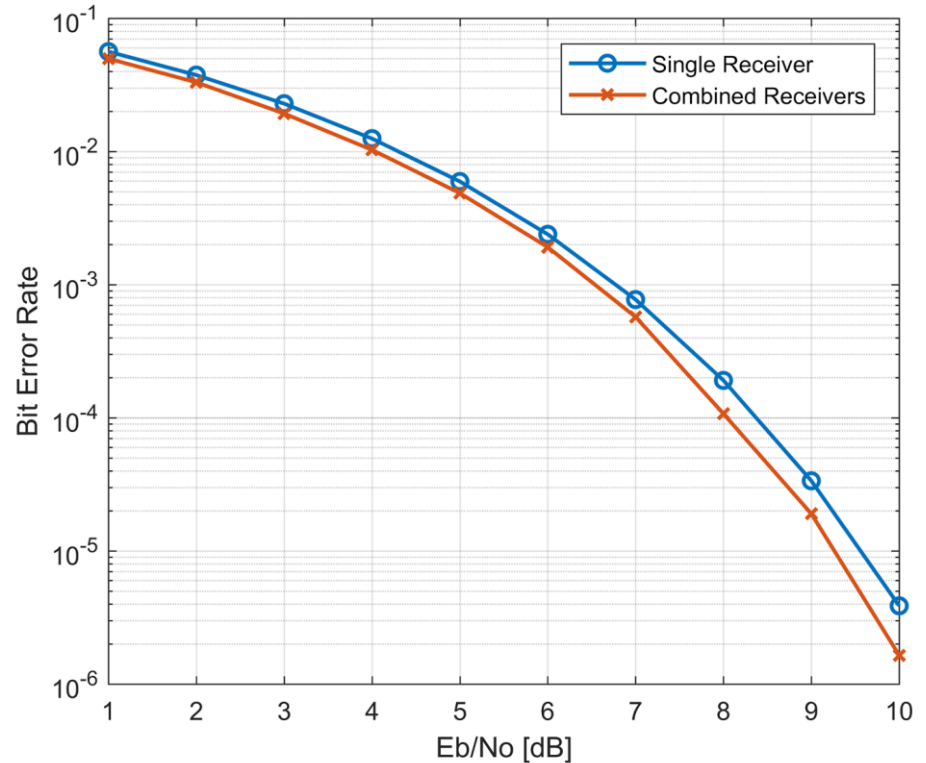
Synchronization in IIOScope



Resulting Bit Error Rate

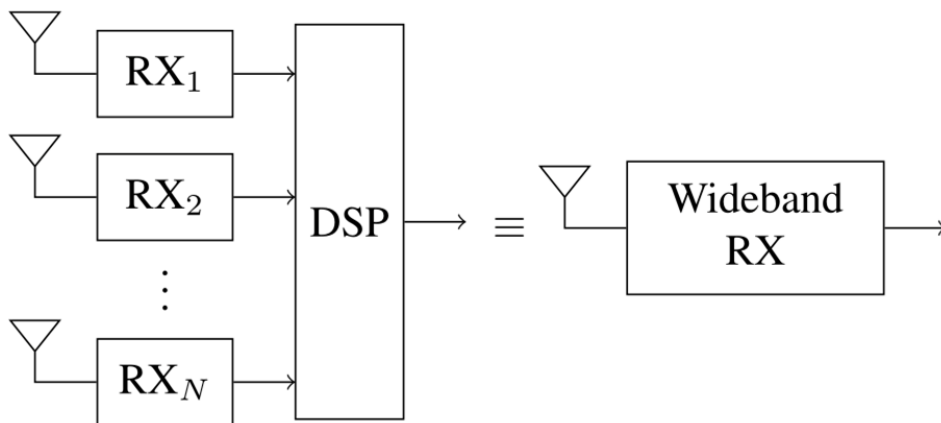
Signal combines coherently, noise combines incoherently.

Increased SNR in overlapping region overcomes implementation loss.



Conclusion

- This is a feasible arbitrary bandwidth radio architecture
- Relatively simple signal processing is used to combine signals
 - Can operate in real-time on an FPGA
- Proven on Rx side, this technique could be turned around for Tx



Questions?